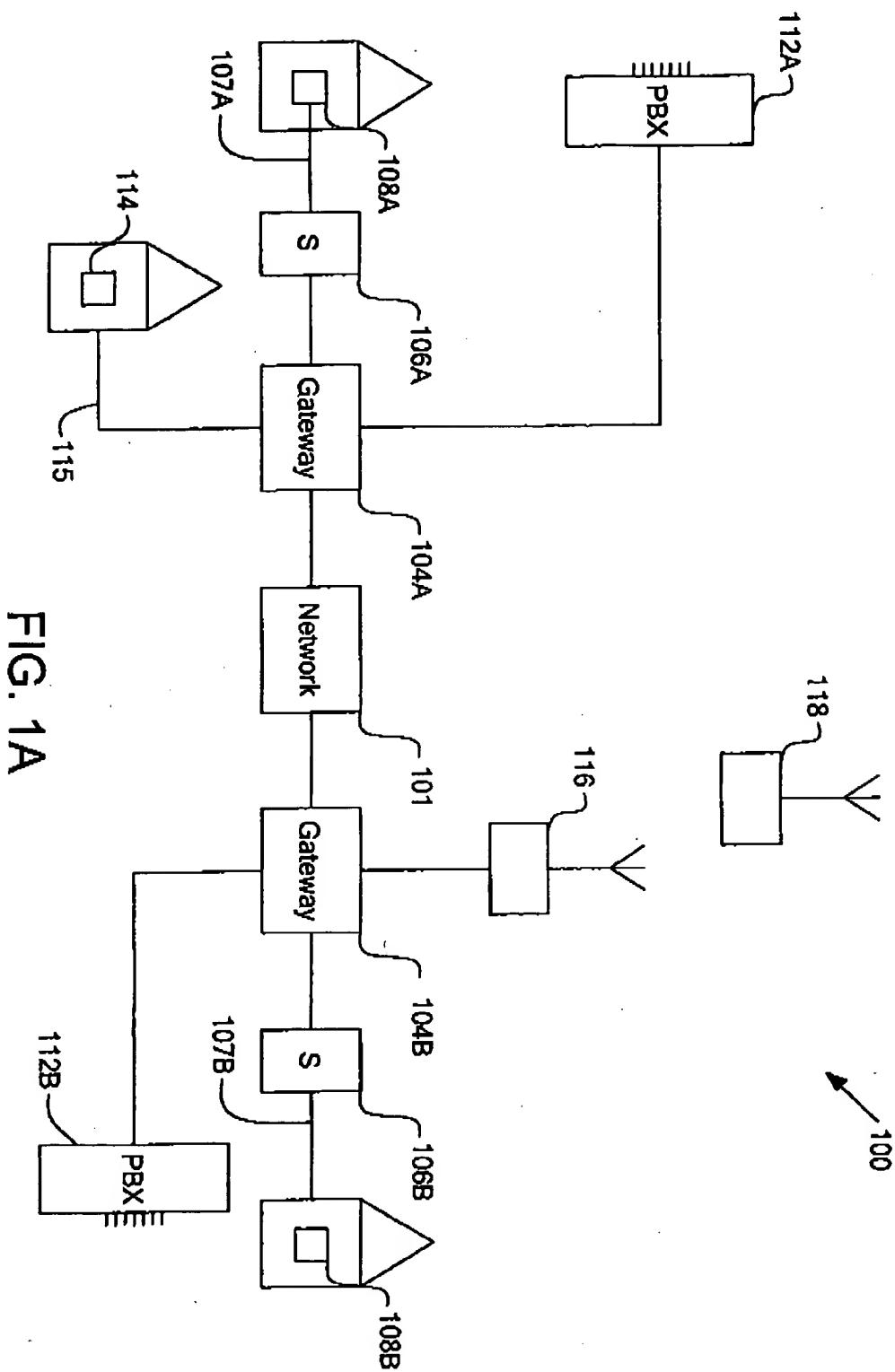


*Attorney Docket No.: 42.P12534  
Application No.: 09/938,104  
Page 2*

***IN THE DRAWINGS:***

***Please replace the originally filed Figs. 1-18 with the replacement Figs. 1-18 filed  
herewith.***

Replacement Sheet 09/938/04



Replacement Sheet 09/938 104

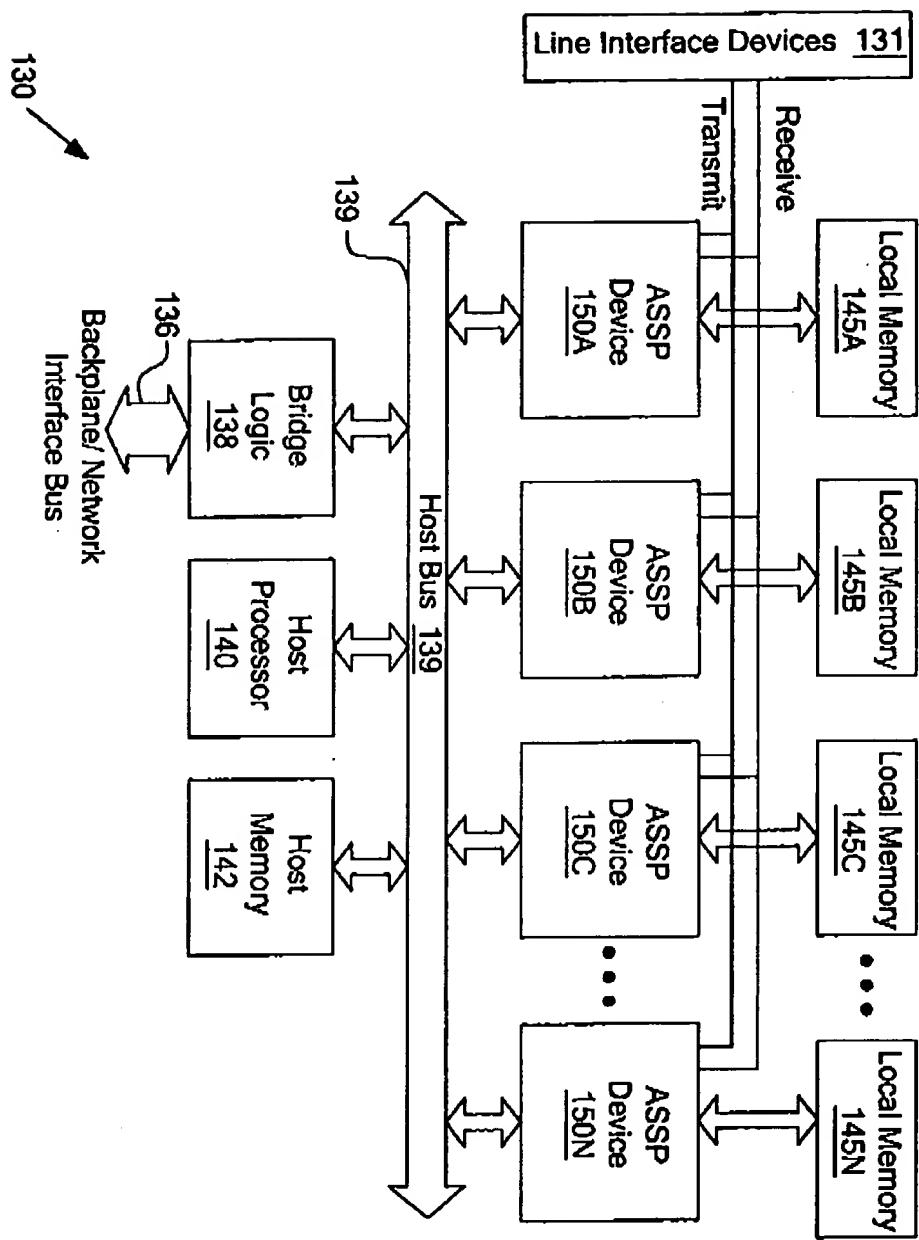


FIG. 1B

Replacement Sheet 09/938 104

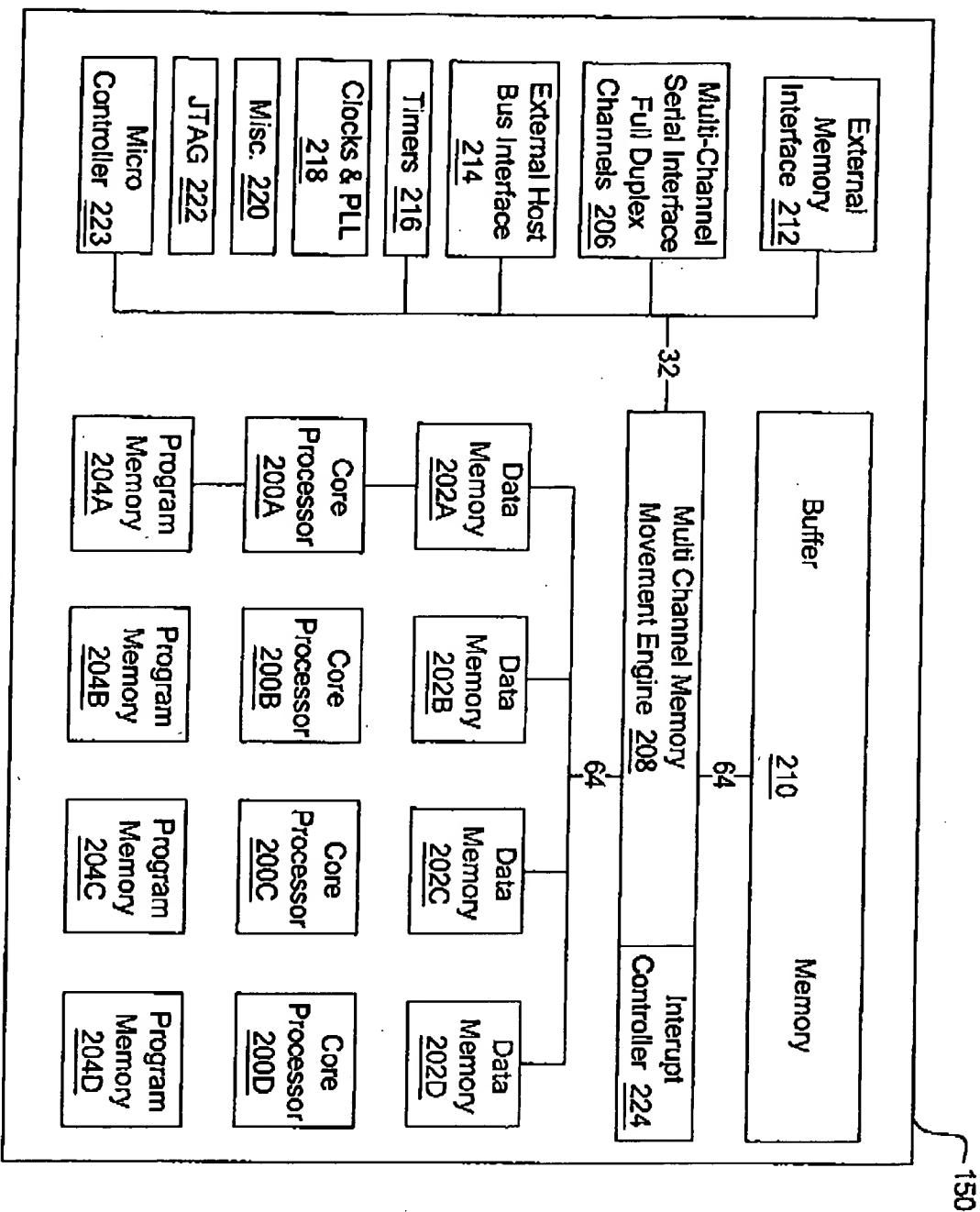


FIG. 2

Replacement Sheet 09/938/104

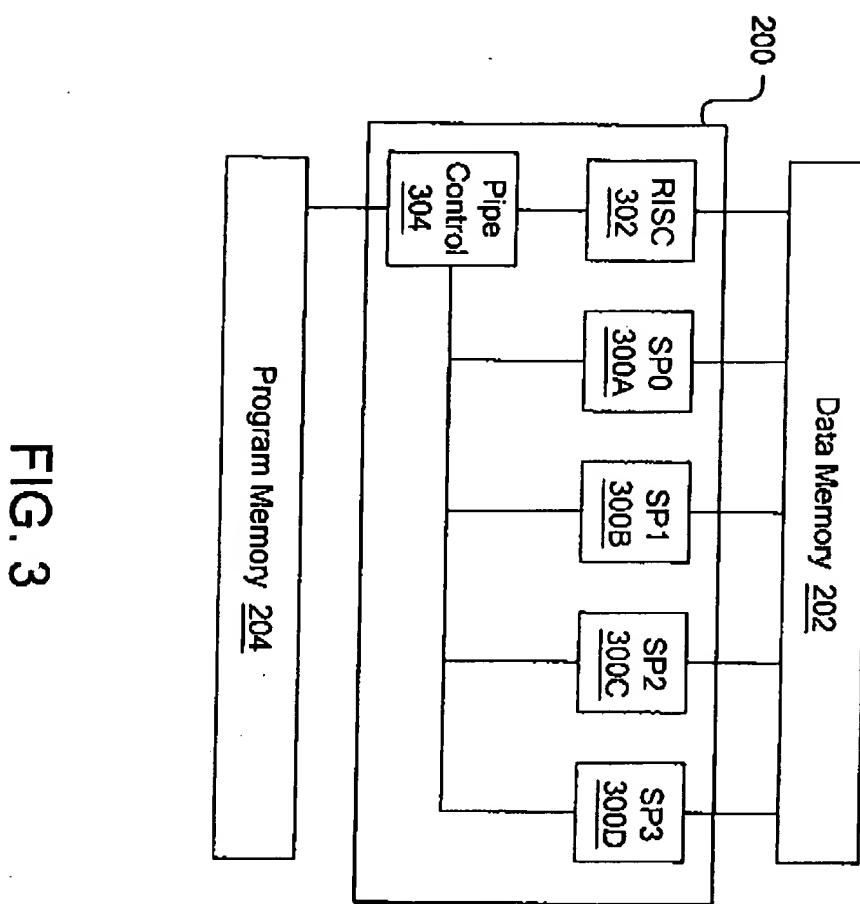


FIG. 3

Replacement Sheet 09/938/04

302

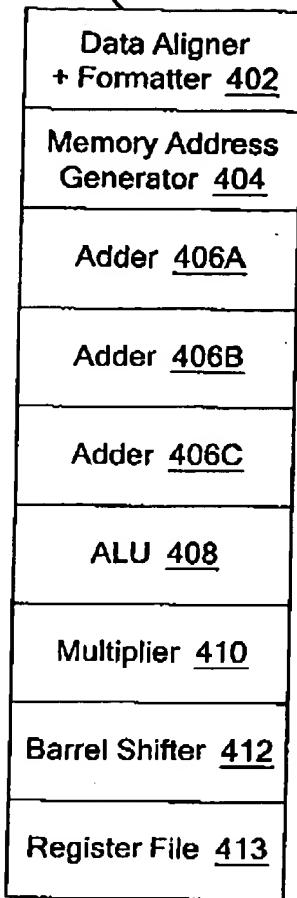


FIG. 4

300

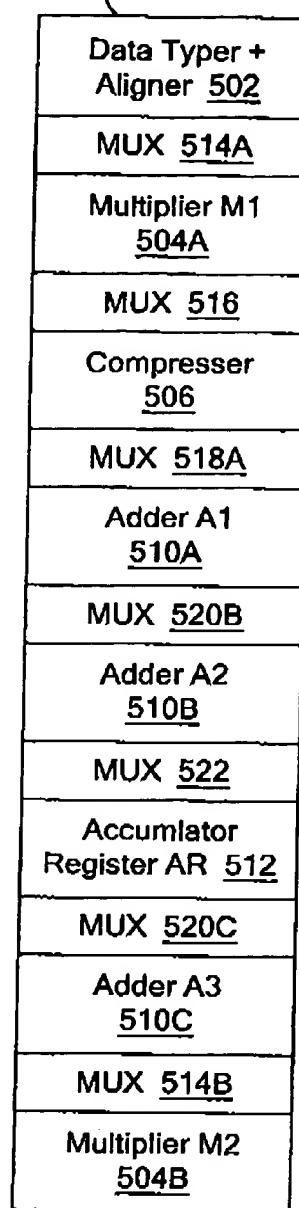


FIG. 5A

Replacement Sheet 09/938 104

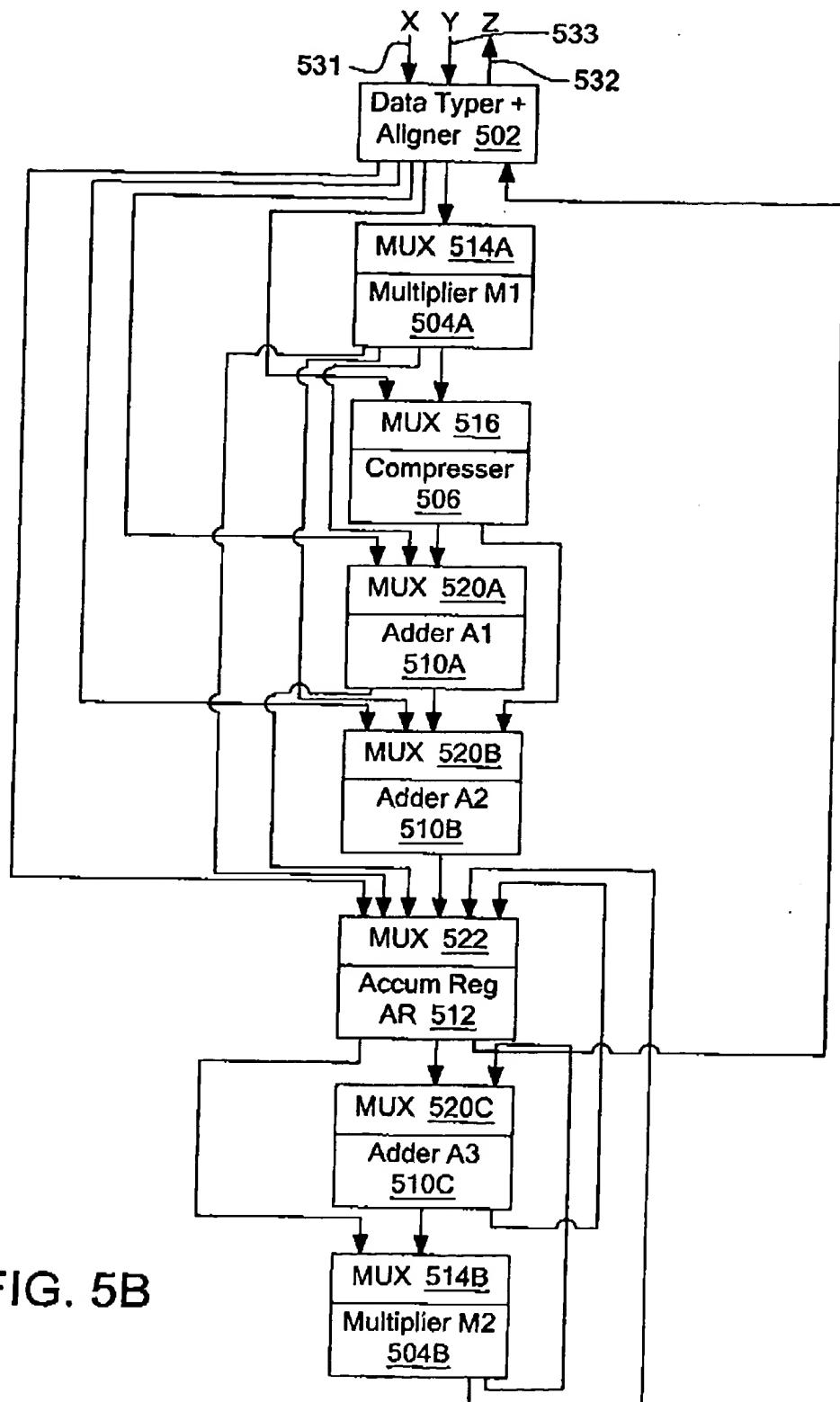


FIG. 5B

Replacement Sheet 09/938104

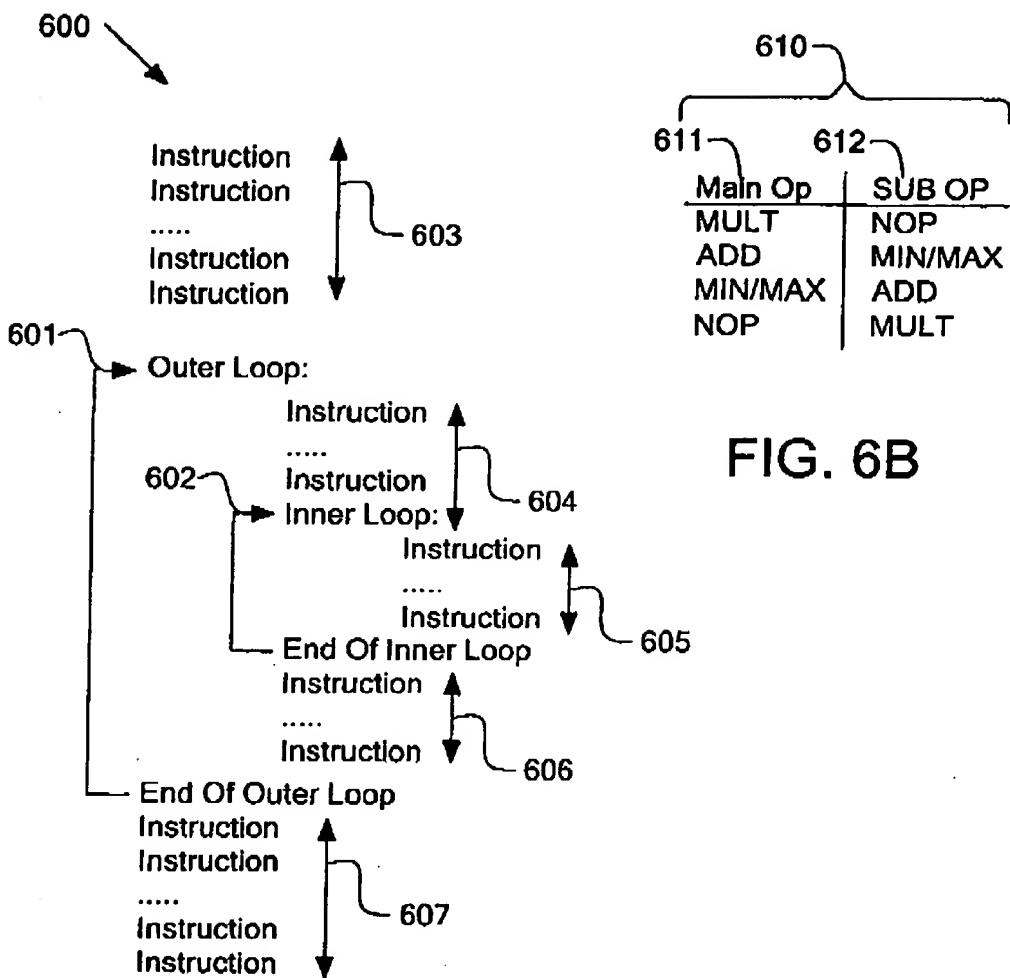


FIG. 6B

FIG. 6A

Replacement Sheet 09/938 104

32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799	800	801	802	803	804	805	806	807	808	809	8010	8011	8012	8013	8014	8015	8016	8017	8018	8019	8020	8021	8022	8023	8024	8025	8026	8027	8028	8029	8030	8031	8032	8033	8034	8035	8036	8037	8038	8039	8040	8041	8042	8043	8044	8045	8046	8047	8048	8049	8050	8051	8052	8053	8054	8055	8056	8057	8058	8059	8060	8061	8062	8063	8064	8065	8066	8067	8068	8069	8070	8071	8072	8073	8074	8075	8076	8077	8078	8079	8080	8081	8082	8083	8084	8085	8086	8087	8088	8089	8090	8091	8092	8093	8094	8095	8096	8097	8098	8099	80100	80101	80102	80103	80104	80105	80106	80107	80108	80109	80110	80111	80112	80113	80114	80115	80116	80117	80118	80119	80120	80121	80122	80123	80124	80125	80126	80127	80128	80129	80130	80131	80132	80133	80134	80135	80136	80137	80138	80139	80140	80141	80142	80143	80144	80145	80146	80147	80148	80149	80150	80151	80152	80153	80154	80155	80156	80157	80158	80159	80160	80161	80162	80163	80164	80165	80166	80167	80168	80169	80170	80171	80172	80173	80174	80175	80176	80177	80178	80179	80180	80181	80182	80183	80184	80185	80186	80187	80188	80189	80190	80191	80192	80193	80194	80195	80196	80197	80198	80199	80200	80201	80202	80203	80204	80205	80206	80207	80208	80209	80210	80211	80212	80213	80214	80215	80216	80217	80218	80219	80220	80221	80222	80223	80224	80225	80226	80227	80228	80229	80230	80231	80232	80233	80234	80235	80236	80237	80238	80239	80240	80241	80242	80243	80244	80245	80246	80247	80248	80249	80250	80251	80252	80253	80254	80255	80256	80257	80258	80259	80260	80261	80262	80263	80264	80265	80266	80267	80268	80269	80270	80271	80272	80273	80274	80275	80276	80277	80278	80279	80280	80281	80282	80283	80284	80285	80286	80287	80288	80289	80290	80291	80292	80293	80294	80295	80296	80297	80298	80299	80300	80301	80302	80303	80304	80305	80306	80307	80308	80309	80310	80311	80312	80313	80314	80315	80316	80317	80318	80319	80320	80321	80322	80323	80324	80325	80326	80327	80328	80329	80330	80331	80332	80333	80334	80335	80336	80337	80338	80339	80340	80341	80342	80343	80344	80345	80346	80347	80348	80349	80350	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20-bit parallel	Control # Control
20-bit serial	Control # Control
40-bit extended	DSP, extensions/Shadow
20-bit serial	DSP # DSP

Control || Control  
Control # Control  
DSP, extensions\Shadow  
DSP # DSP

DSP Instructions

Multiply	29	39	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20
1    0    0    PS	S <sup>0</sup>	S <sup>1</sup>	S <sup>2</sup>	S <sup>3</sup>	S <sup>4</sup>	S <sup>5</sup>	S <sup>6</sup>	S <sup>7</sup>	S <sup>8</sup>	S <sup>9</sup>	S <sup>10</sup>	S <sup>11</sup>	S <sup>12</sup>	S <sup>13</sup>	S <sup>14</sup>	S <sup>15</sup>	S <sup>16</sup>	S <sup>17</sup>	S <sup>18</sup>	

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Replacement Sheet 09/938104

## Control and Specifier Extensions

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

Mul

0	Pred	PL	Sxt	Sy	Rnd	1	S	S	S	0	SA	DA	abs	0	0				
---	------	----	-----	----	-----	---	---	---	---	---	----	----	-----	---	---	--	--	--	--

Add/Sub

min/max

Gx

0	Pred	PL	Sxt	Sy	LI	Subext	0	SA	DA	abs	0	0							
---	------	----	-----	----	----	--------	---	----	----	-----	---	---	--	--	--	--	--	--	--

Add/Sub

Mul

+L	+H	+L	X																
----	----	----	---	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

Vis

Rnd

Vis

X	VS	Rnd	Fp																
---	----	-----	----	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

Inc/

Gx

Fp

0	Pred	PL	Sxt	Sy	LI	Gx	Subext	0	SA	DA	abs	0	0						
---	------	----	-----	----	----	----	--------	---	----	----	-----	---	---	--	--	--	--	--	--

Add/Sub

Mul

LI	Fp																		
----	----	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

Vis

Rnd

Vis

0	Pred	PL	Sxt	Sy	PC11	0	ereg	PC11	0	0									
---	------	----	-----	----	------	---	------	------	---	---	--	--	--	--	--	--	--	--	--

Add/Sub

Mul

0

ereg

PC11

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Refluent Sheet 09/938 104

add,sub	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
max,min	l	Pred	0	0	0	0	0	RX			RY			RZ		RZ		RZ		RZ
Shift	l	Pred	0	0	0	1		RX			RY			RZ		RZ		XIN		0
Logic	l	Pred	0	1	0			RX			RY			RZ		RZ		0		0
Mux	l	Pred	0	1	1			RX			RY			RZ		RZ		0		0
mov	l	Pred	0	1	1			RX			RY			RZ		RZ		XIN		1
add	l	Pred	0	1	1			RX			RY			RZ		RZ		0		0
movZero	l	Pred	0	1	1			RX			RY			RZ		RZ		0		0
Ldm	l	Pred	0	1	1			RX			RY			RZ		RZ		0		0
bits	l	Pred	0	1	1			RX			RY			RZ		RZ		0		0
bts	l	Pred	1	0	0			RX			RY			RZ		RZ		0		0
Setbit	l	Pred	1	0	0			RX			RY			RZ		RZ		0		0
Movt	l	Pred	1	0	0			RX			RY			RZ		RZ		0		0
Jmp	l	Pred	1	0	1			RX			RY			RZ		RZ		0		0
Call	l	Pred	1	0	1			RX			RY			RZ		RZ		0		0
Loop	l	Pred	1	0	1			RX			RY			RZ		RZ		0		0
Jmpl	l	Pred	1	0	1			RX			RY			RZ		RZ		0		0
Call	l	Pred	1	0	1			RX			RY			RZ		RZ		0		0
Loopi	l	Pred	1	0	1			RX			RY			RZ		RZ		0		0
Test	l	Pred	1	1	0			RX			RY			RZ		RZ		0		0
Testbit	l	Pred	1	1	0			RX			RY			RZ		RZ		0		0
AndOp, OrOp	l	Pred	1	1	0			RX			RY			RZ		RZ		0		0
Load	l	Pred	1	1	0			RX			RY			RZ		RZ		0		0
Store	l	Pred	1	1	1			RX			RY			RZ		RZ		0		0
Aligned	l	Pred	1	1	1			RX			RY			RZ		RZ		0		0
Store	l	Pred	1	1	1			RX			RY			RZ		RZ		0		0
Extended	l	Pred	1	1	1			RX			RY			RZ		RZ		0		0
Logic2	l	Pred	1	1	1			RX			RY			RZ		RZ		0		0
movtEq	l	Pred	1	1	1			RX			RY			RZ		RZ		0		0
Crc	l	Pred	1	1	1			RX			RY			RZ		RZ		0		0
Parity	l	Pred	1	1	1			RX			RY			RZ		RZ		0		0
Sim	l	Pred	1	1	1			RX			RY			RZ		RZ		0		0
Abs	l	Pred	1	1	1			RX			RY			RZ		RZ		0		0
Neg	l	Pred	1	1	1			RX			RY			RZ		RZ		0		0
DivStep	l	Pred	1	1	1			RX			RY			RZ		RZ		0		0
Set	l	Pred	1	1	1			RX			RY			RZ		RZ		0		0
Resigned	l	Pred	1	1	1			RX			RY			RZ		RZ		0		0
Return	l	Pred	1	1	1			RX			RY			RZ		RZ		0		0
Sync	l	Pred	1	1	1			RX			RY			RZ		RZ		0		0
Swi	l	Pred	1	1	1			RX			RY			RZ		RZ		0		0
Nop	l	Pred	1	1	1			RX			RY			RZ		RZ		0		0

&lt;Bit1, Bits2-4&gt; == UI5 [Shift Amount]

FIG. 6F

Replacement Sheet 09/938104

Extended Control

		Insert/Extract									
		13-12					13-12 of upper half (38-20)				
		R2		R2			R2		R2		
Register	Op	R2	R2	R2	R2	R2	R2	R2	R2	R2	R2
jmp, call	U17	U17	U17	U17	U17	U17	U17	U17	U17	U17	U17
dbnop	U14:outer LC	U14:inner LC	0	0	1	1	0	0	0	0	0
loop	R2	R2	0	0	1	1	0	x			
l1	R2	R2	0	1	0	0	0	x			
sub	R2	R2	0	1	0	0	0	x			
Reserved	R2	R2	0	0	1	0	0	x			
logrep	R2	R2	0	0	0	0	0	x			
Test	R2	D	R2	D	1	0	1	0			
Move	HL	HL	R2	0	1	1	0	0	x		
Load	Type	Type	0	1	1	0	x				
Store	R2	R2	0	1	1	0	x				
Load	R2	R2	0	1	1	1	0	x			
Store	R2	R2	0	1	1	1	0	x			
Add/Subtr	R2	R2	1	0	1	0	0	x			
Mul/Div	R2	R2	1	0	x	1	0	x			
Add/Subtr	R2	R2	1	0	x	1	0	x			

PAGE 10/34 \* RCVD AT 12/2/2004 11:50:10 PM [Eastern Standard Time] \* SVR:USPTO-EFXRF-1/0 \* DNIS:8729306 \* CSID:703476 5664 \* DURATION (mm:ss):18-30

## Replace Sheet 09/938 104

MAC:

39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	PL	PS	Subop	Rnd L1 Vis S+ DA SA =+ Control
Group Pred opcode				
149 bit				
2-20 bit				

res

ARITH:

39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	PL	PS	Rnd S* DA VIS LI S* S* S*	MUL-NOP
Group Pred opcode				
0 0 NOP	PL	PS	Rnd S* DA VIS LI S* S* S*	MUL-ADD
0 1 Acc	PL	PS	Rnd S* DA VIS LI =+ S* NM	MUL-EXT

EXT:

39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	PL	PS	Rnd S* DA VIS LI =+ S* SA	MUL-MUL
Group Pred opcode				
0 0 NOP	PL	PS	Rnd S* DA VIS LI =+ S* SA	MUL-MUL
0 1 Acc	PL	PS	Rnd S* DA VIS LI =+ S* SA	MUL-MUL

LOGIC:

39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	PL	PS	Rnd S* DA VIS LI =+ S* SA	
Group Pred opcode				
0 0 NOP	PL	PS	Rnd S* DA VIS LI =+ S* SA	
0 1 Acc	PL	PS	Rnd S* DA VIS LI =+ S* SA	

IMM:

39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	PL	PS	Rnd S* DA VIS LI =+ S* SA	
Group Pred opcode				
0 0 NOP	PL	PS	Rnd S* DA VIS LI =+ S* SA	
0 1 Acc	PL	PS	Rnd S* DA VIS LI =+ S* SA	

IMMEDIATE:

39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	PL	PS	Rnd S* DA VIS LI =+ S* SA	
Group Pred opcode				
0 0 NOP	PL	PS	Rnd S* DA VIS LI =+ S* SA	
0 1 Acc	PL	PS	Rnd S* DA VIS LI =+ S* SA	

Test:

39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	PL	PS	Rnd S* DA VIS LI =+ S* SA	
Group Pred opcode				
0 0 NOP	PL	PS	Rnd S* DA VIS LI =+ S* SA	
0 1 Acc	PL	PS	Rnd S* DA VIS LI =+ S* SA	

Branch:

39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	PL	PS	Rnd S* DA VIS LI =+ S* SA	
Group Pred opcode				
0 0 NOP	PL	PS	Rnd S* DA VIS LI =+ S* SA	
0 1 Acc	PL	PS	Rnd S* DA VIS LI =+ S* SA	

Misc:

FIG. 6H

## Replacement Sheet 09/938104

## 7-bit specifier: Parallel Store, Parallel Load In DSP Instructions

6	5	4	3	2	1	0
M/R	0	0	0	SPIR p0-p15		
0	0	1		reserved	Mem(p1r)    pir + = kls	Always postupdate
0	1	0		scnames	Mem(p1r + kls)	Always preupdate
0	1	1		ppr: n0-n15		
0	1			pir (0) to (r5)	pir	
1	1			pir si U4	pir	

## 6-bit specifier: DSP Instructions

5	4	3	2	1	0
M/R	0	0	scnames		
0	1		ppr: n0-n15		
1			pir (0) to (r5)	pir	

## 5-bit specifier: RISC Instructions

4	3	2	1	0
0	SPR: p0-p15			
0	ppr: n0-n15			

Always postupdate

## 4-bit specifier:

3	2	1	0
0	SPR: p0-p15		
0	ppr: n0-n15		
0	SPR: p0-p15		

RISC Instructions  
20-bit DSP Instructions  
20-bit Shadow DSP Instructions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
AR																																

Type

permute

C8 ldx(UJ)(0-7)

ldx: S16(-10 to 15)

pir

FIG. 6I1

## Replacement Sheet 09/938/04

eregnames:										sc-names:									
3	0	0	0	0	0	0	0	0	0	A0	(use type, SMD)	ppr-type							
2	0	0	0	0	0	0	0	0	0	A1		ereg-type							
1	0	0	0	0	0	0	0	0	0	T		hi-g							
0	0	0	0	0	0	0	0	0	0	TR		pls-pr							
3	0	0	0	0	0	0	0	0	0	A00	(unit: 0)	cb-cr							
2	0	0	0	0	0	0	0	0	0	A10		loop-dr							
1	0	0	0	0	0	0	0	0	0	TO		pcr							
0	0	0	0	0	0	0	0	0	0	TR0		status							
3	0	0	0	0	0	0	0	0	0	SX1									
2	0	0	0	0	0	0	0	0	0	SX2									
1	0	0	0	0	0	0	0	0	0	SX2s									
0	0	0	0	0	0	0	0	0	0	SY1									
3	0	0	0	0	0	0	0	0	0	SY2									
2	0	0	0	0	0	0	0	0	0	SY1s									
1	0	0	0	0	0	0	0	0	0	SY2s									
0	0	0	0	0	0	0	0	0	0	ST1s									
3	0	0	0	0	0	0	0	0	0	ST2s									
2	0	0	0	0	0	0	0	0	0										
1	0	0	0	0	0	0	0	0	0										
0	0	0	0	0	0	0	0	0	0										

FIG. 612

Replaceent Sheet 09/938 104

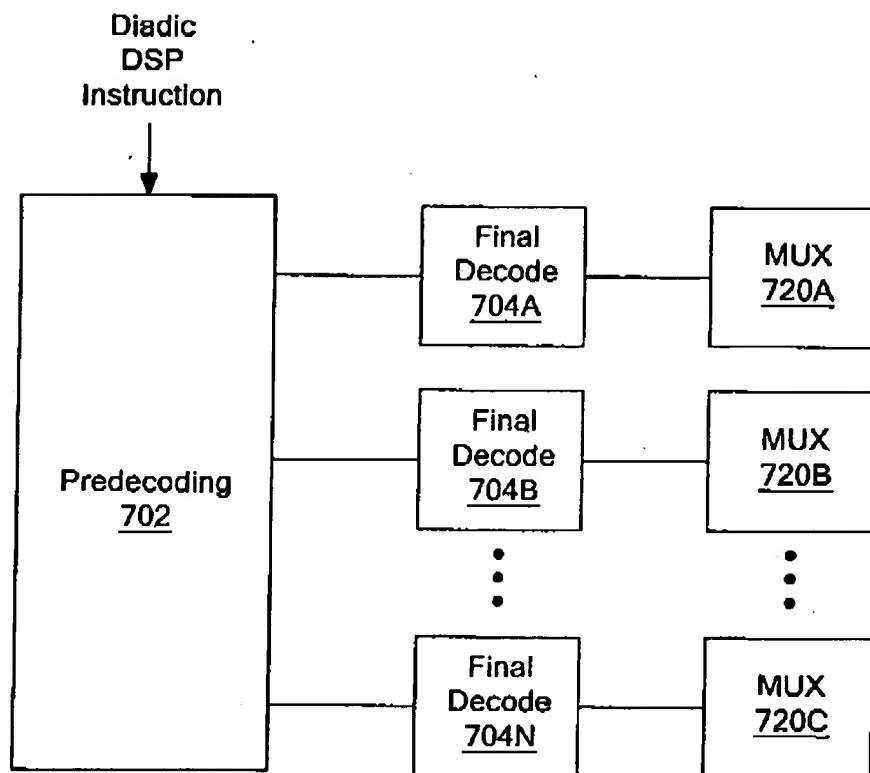


FIG. 7

Replacement Sheet 09/988 104

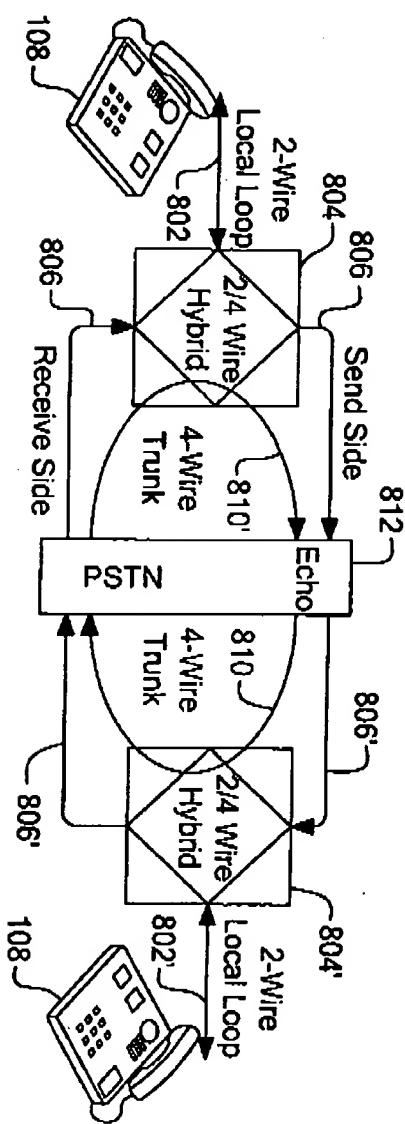


FIG. 8  
(Prior Art)

Replaced Sheet 09/938104

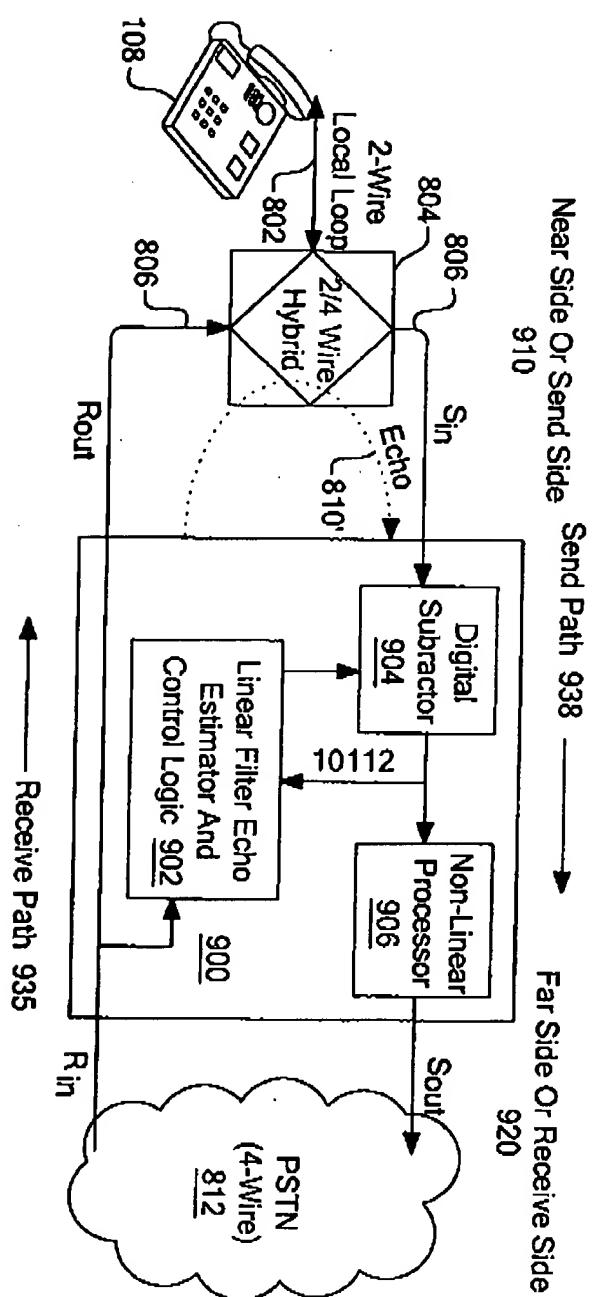


FIG. 9  
(Prior Art)

Replacement Sheet 09/938104

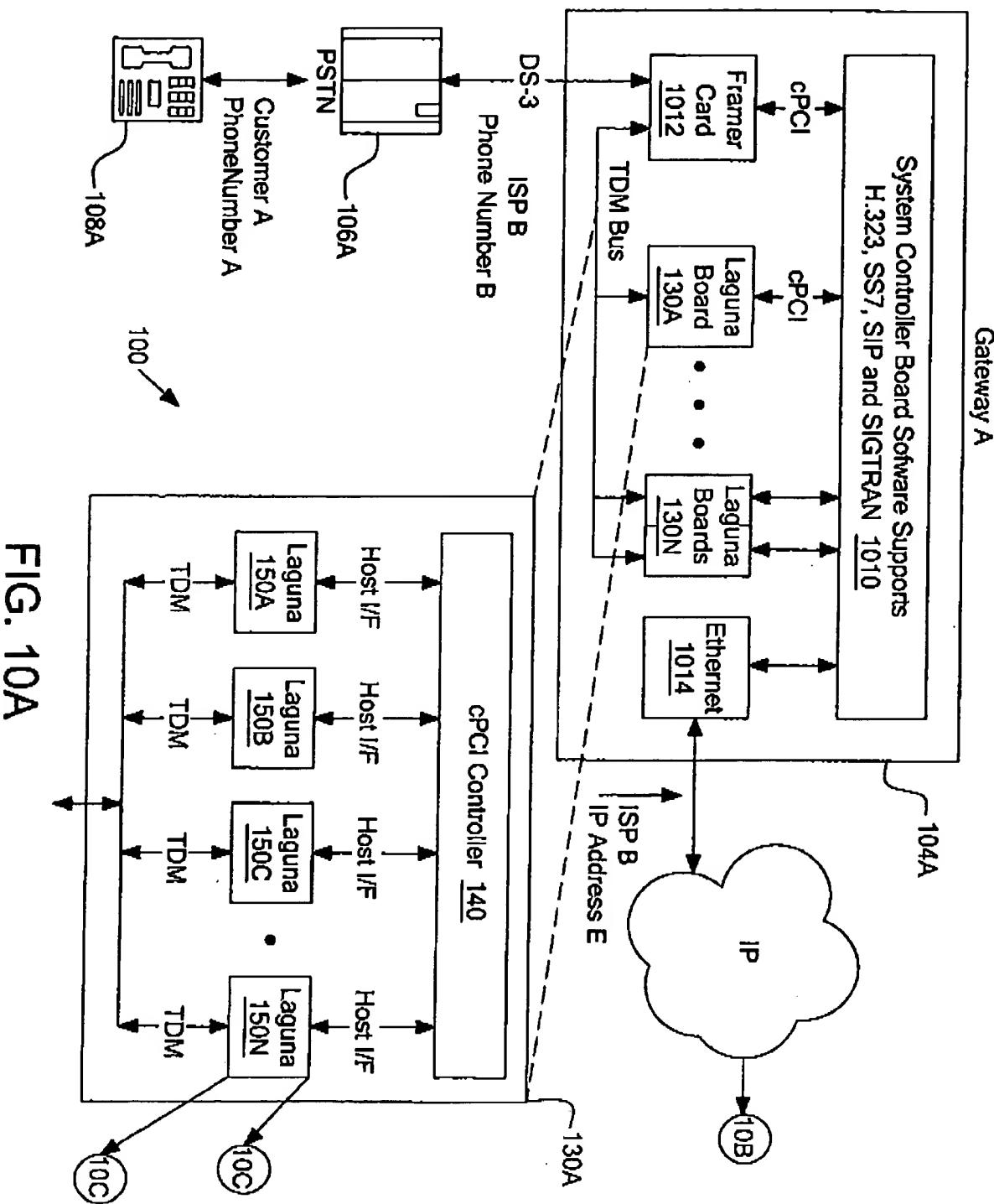


FIG. 10A

Replacement Sheet 09/938104

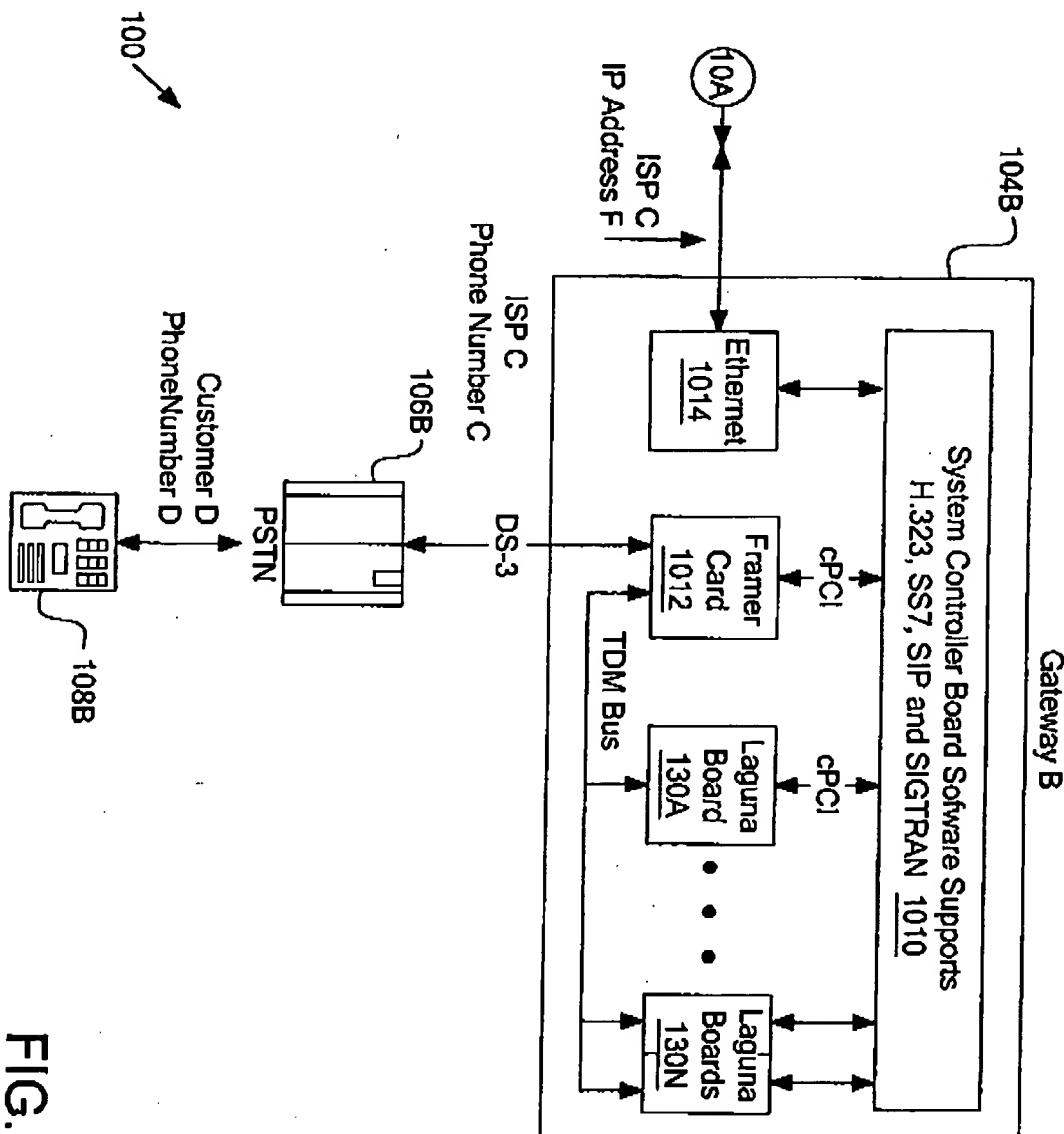
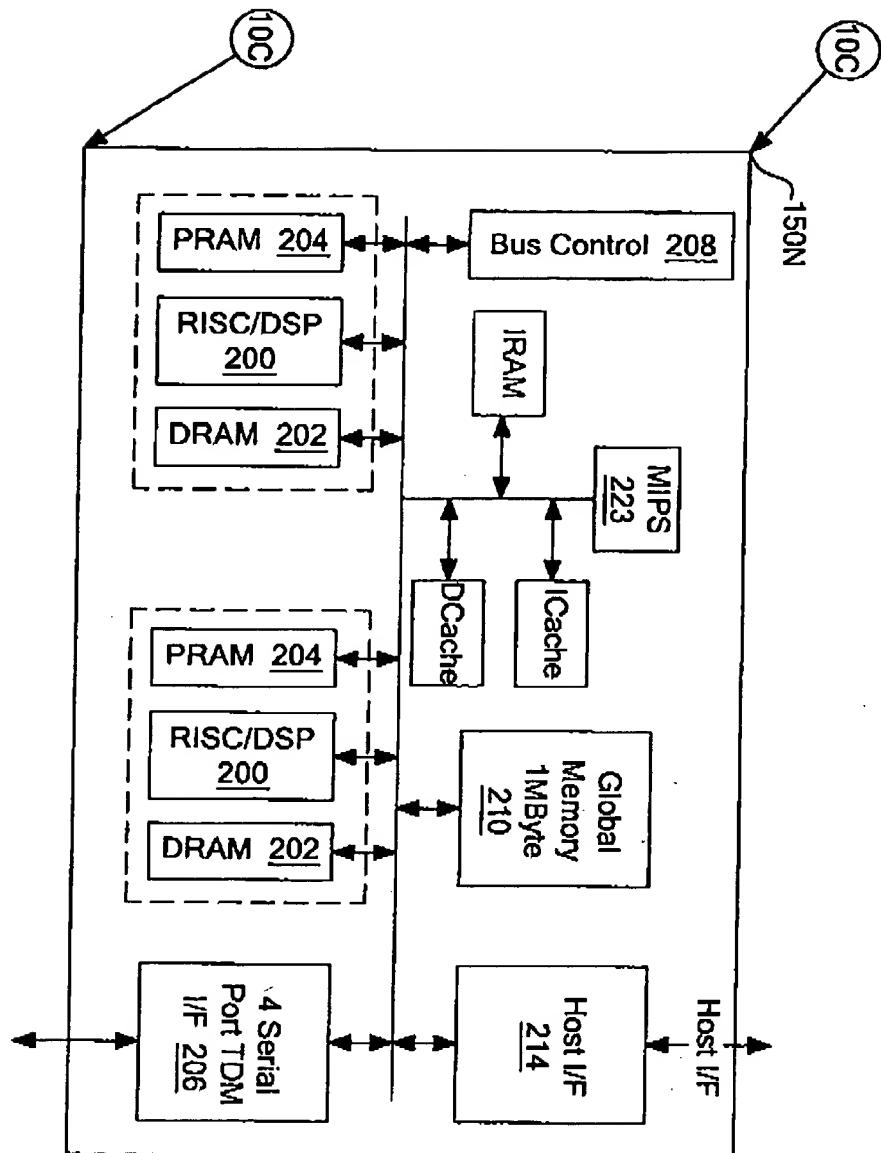
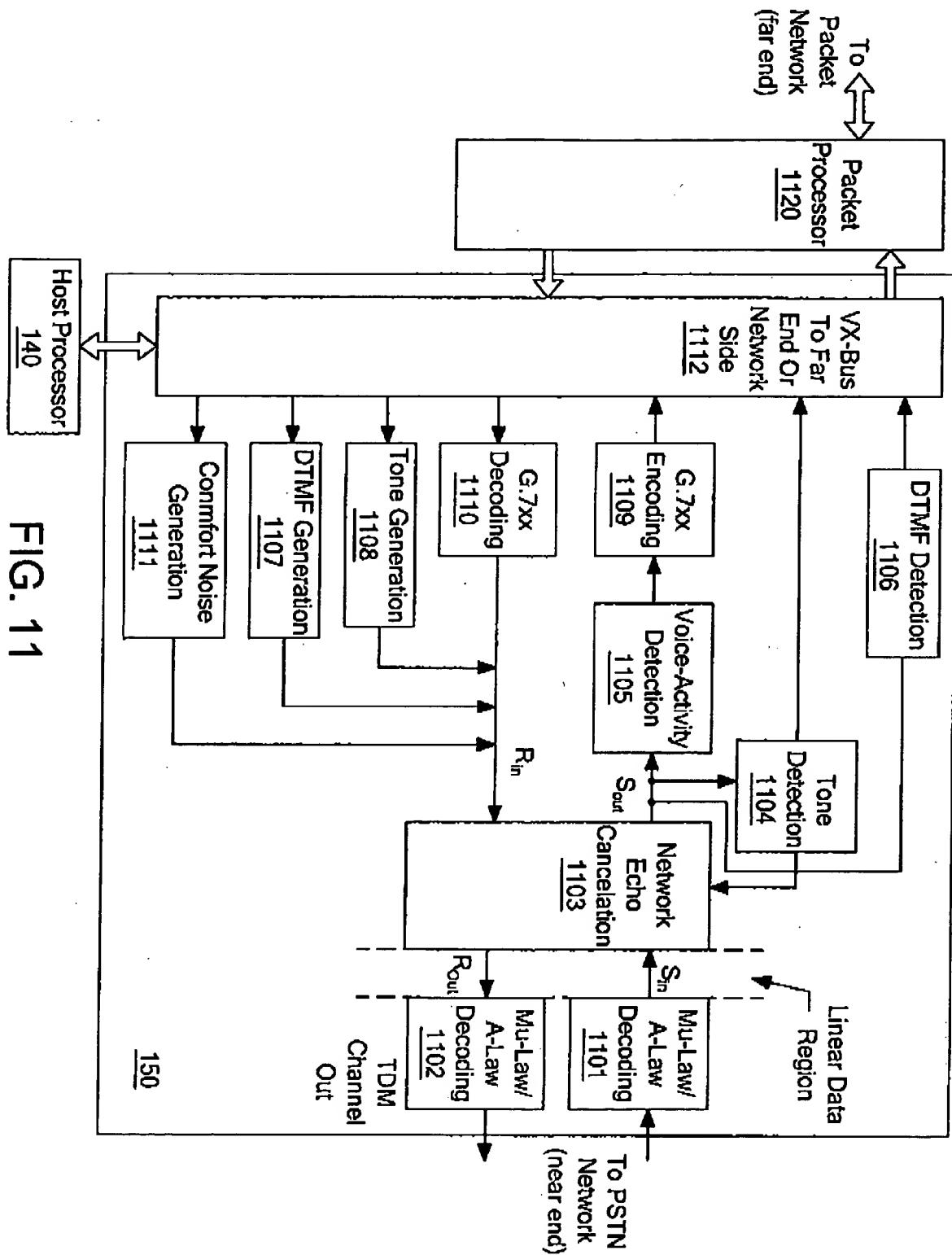


FIG. 10B

Replacement Sheet 09/938 104

100  
10C  
FIG. 10C

Replacement Sheet 09/938 10f



Replacement Sheet 09/938 104

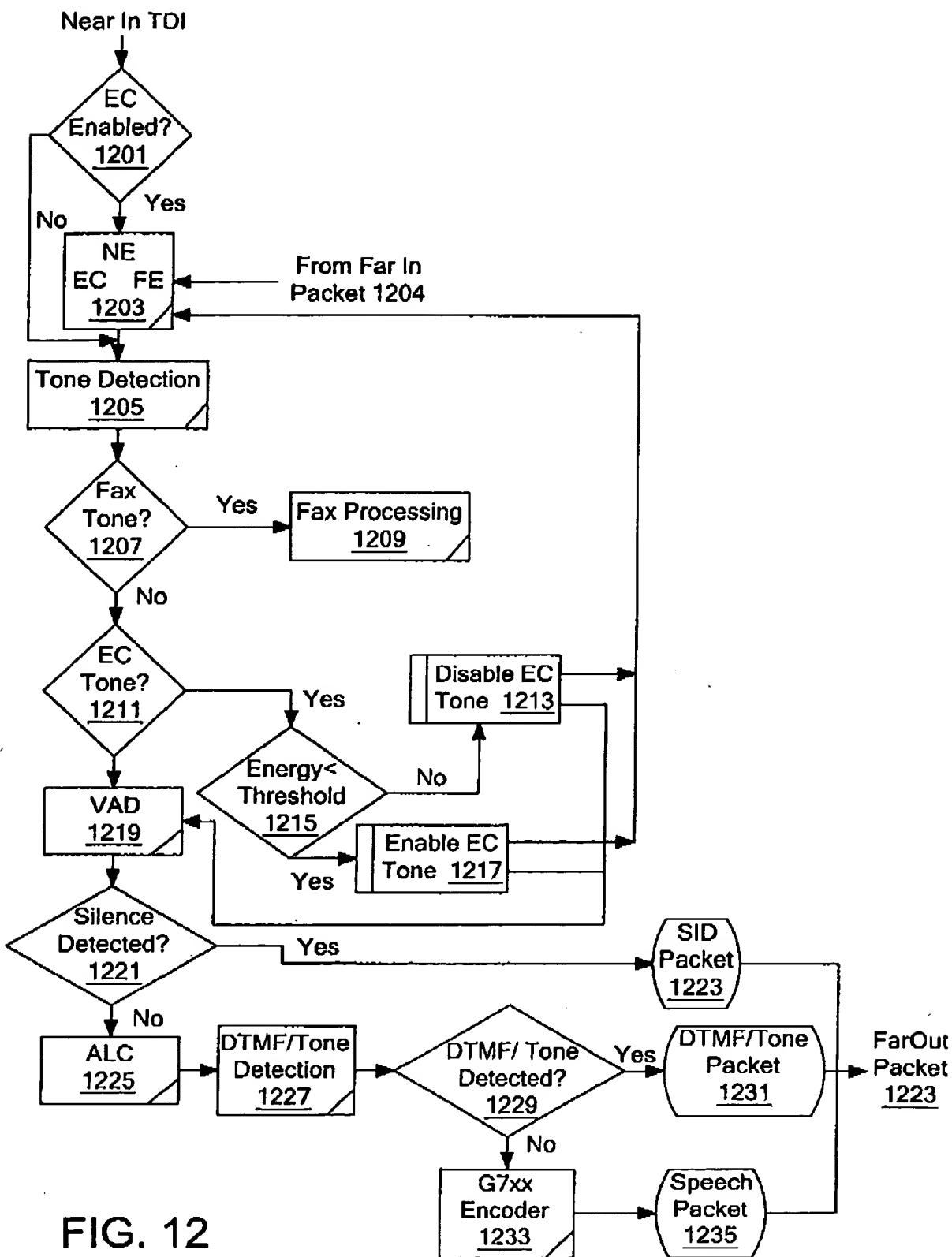


FIG. 12

Replacement Sheet 09/938104

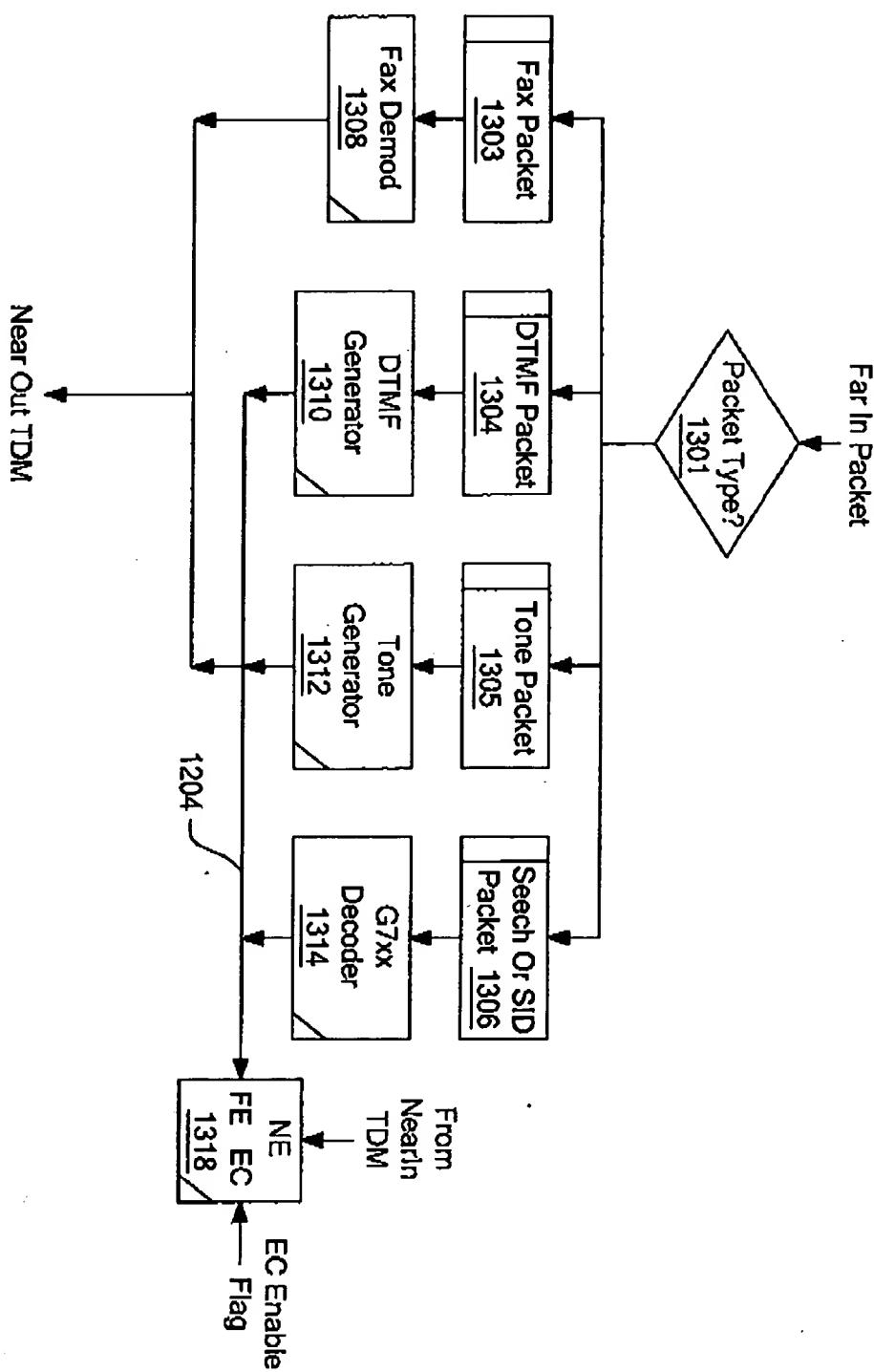


FIG. 13

Replacement Sheet 09/938 104

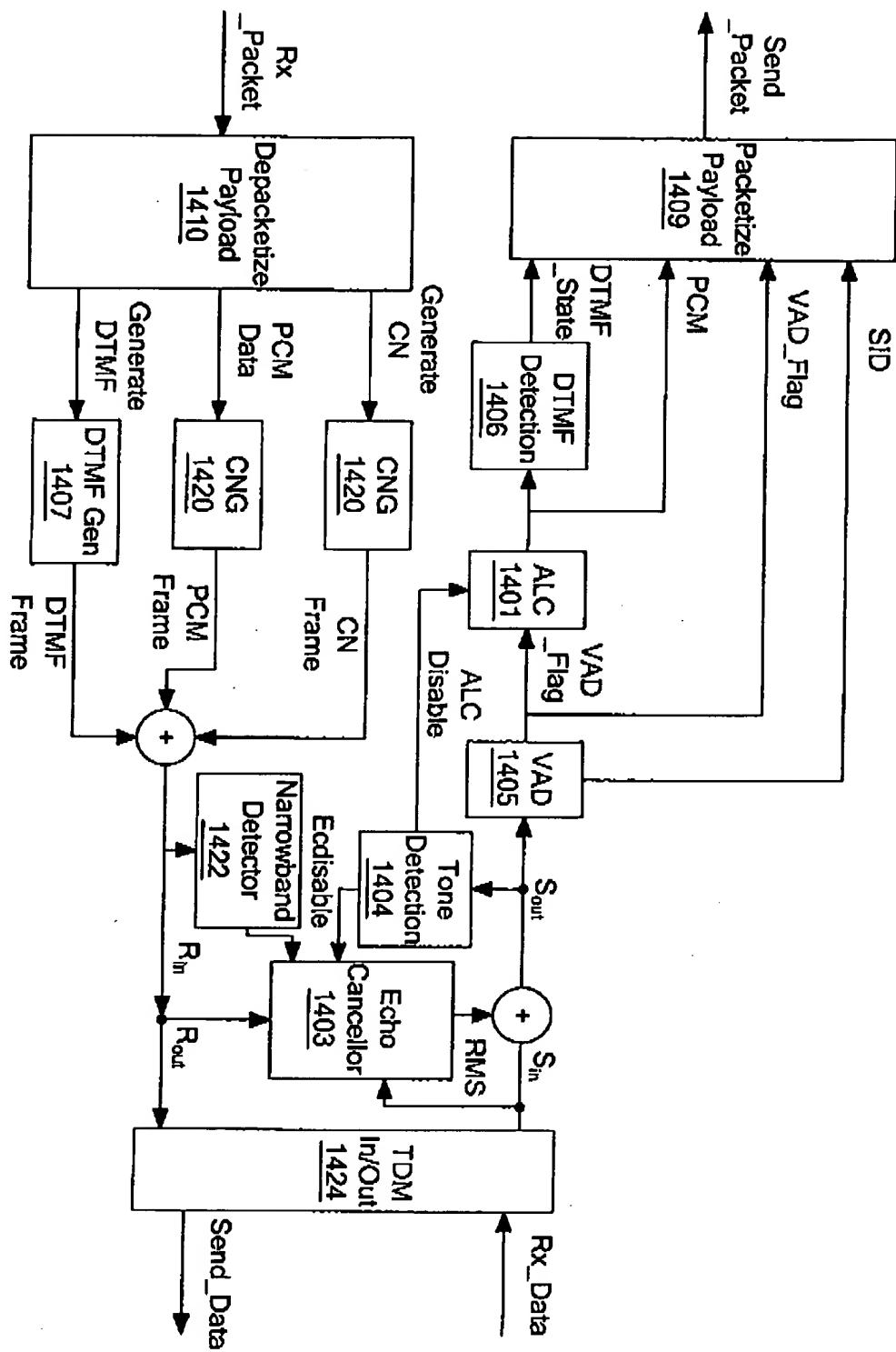


FIG. 14A

Replacement Sheet 09/938 104

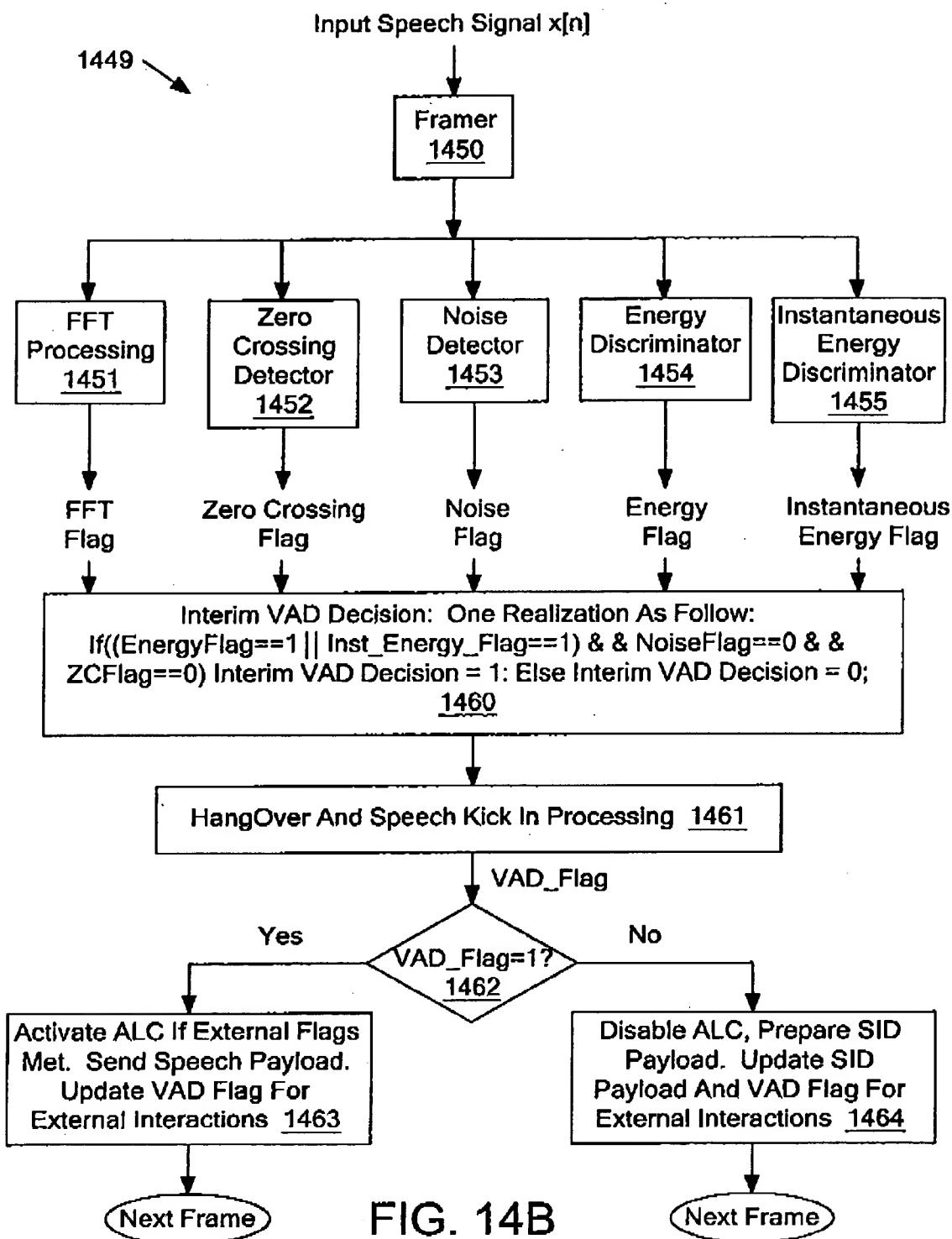


FIG. 14B

Replacement Sheet 09/938104

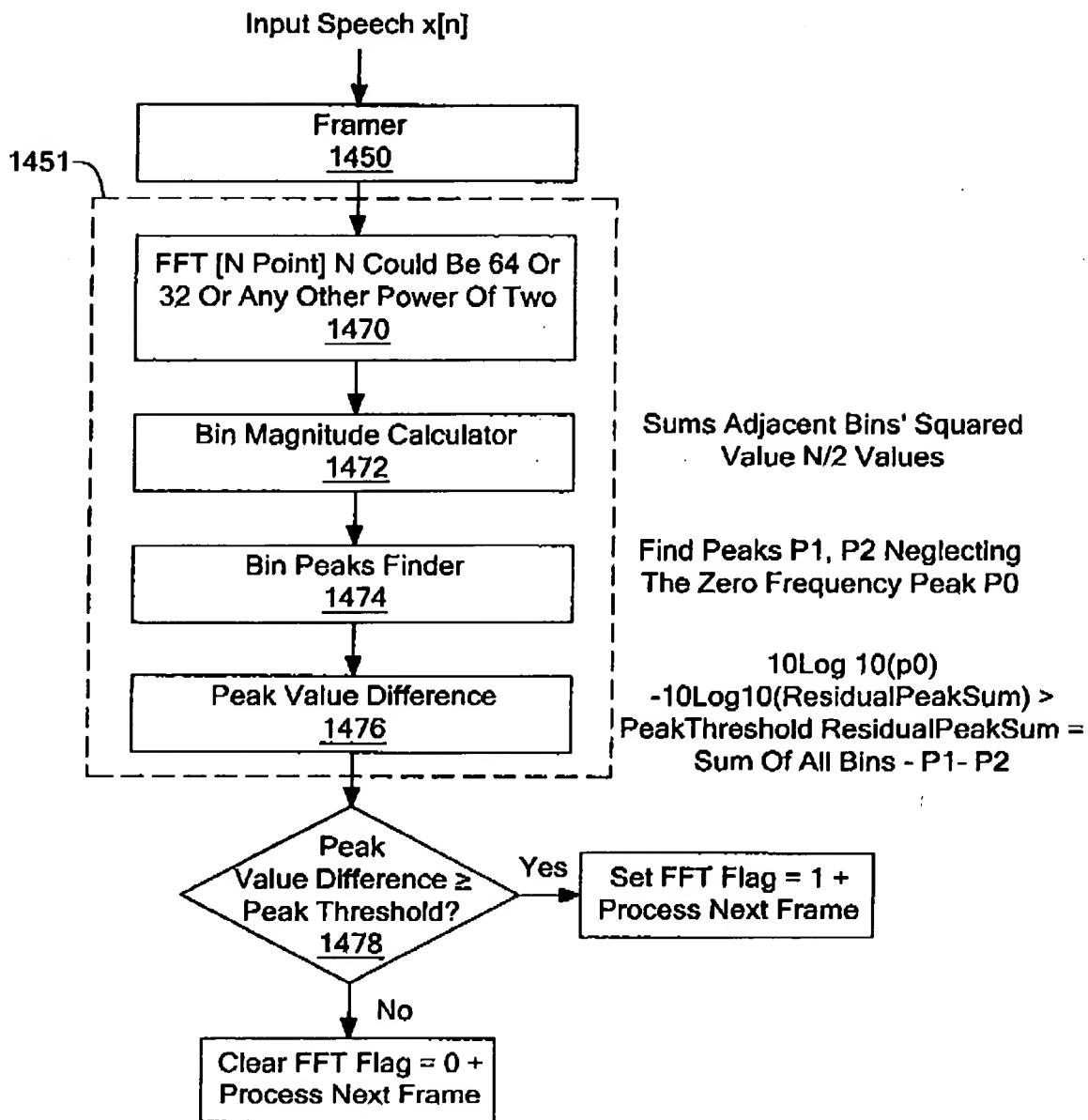
FFT Processing Of Input  
Speech For VAD

FIG. 14C

Replacement Sheet 09/938104

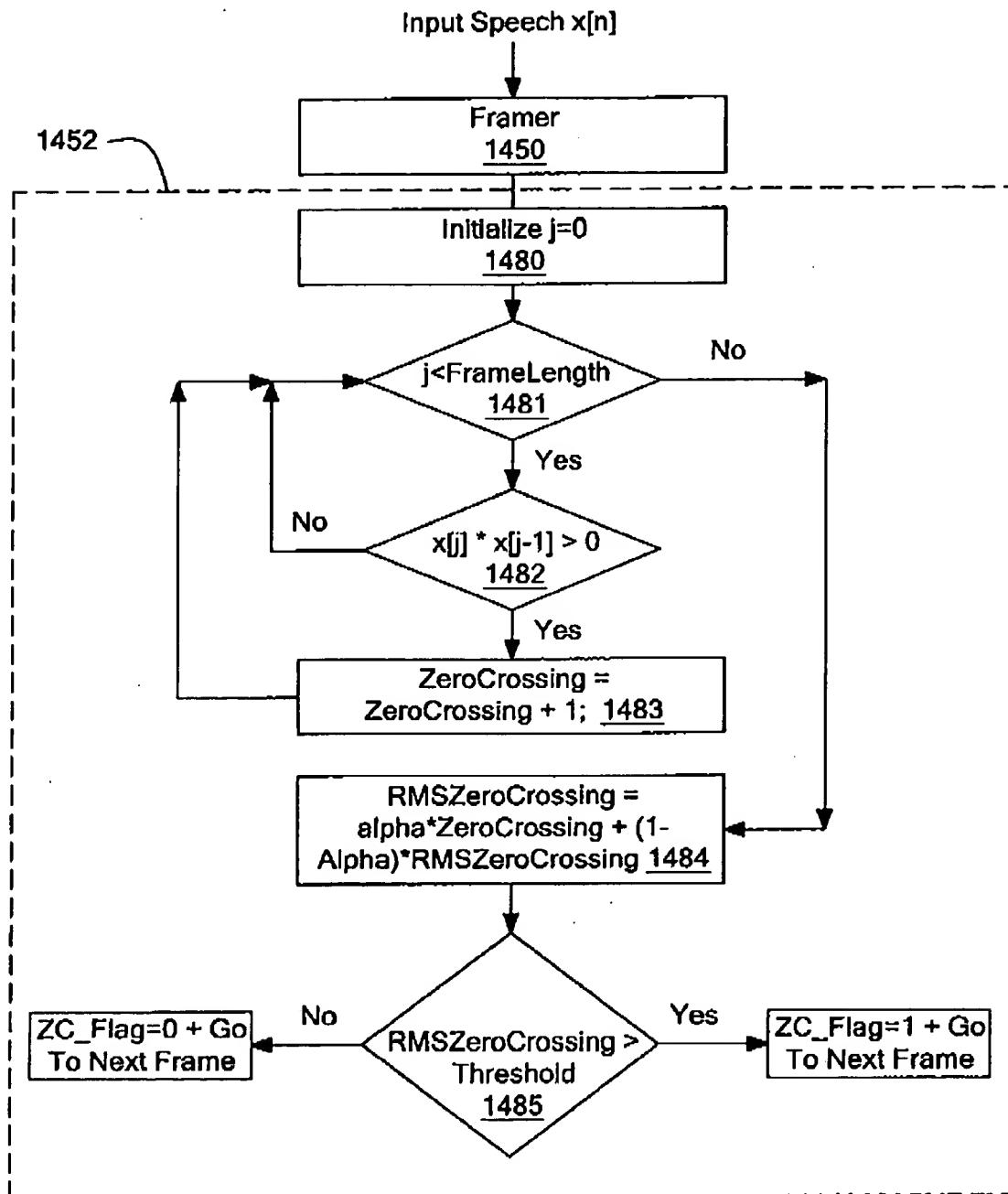
Zero Crossing Detector 1452

FIG. 14D

Replacement Sheet 09/938 104

## Noise Detection In VAD 1453

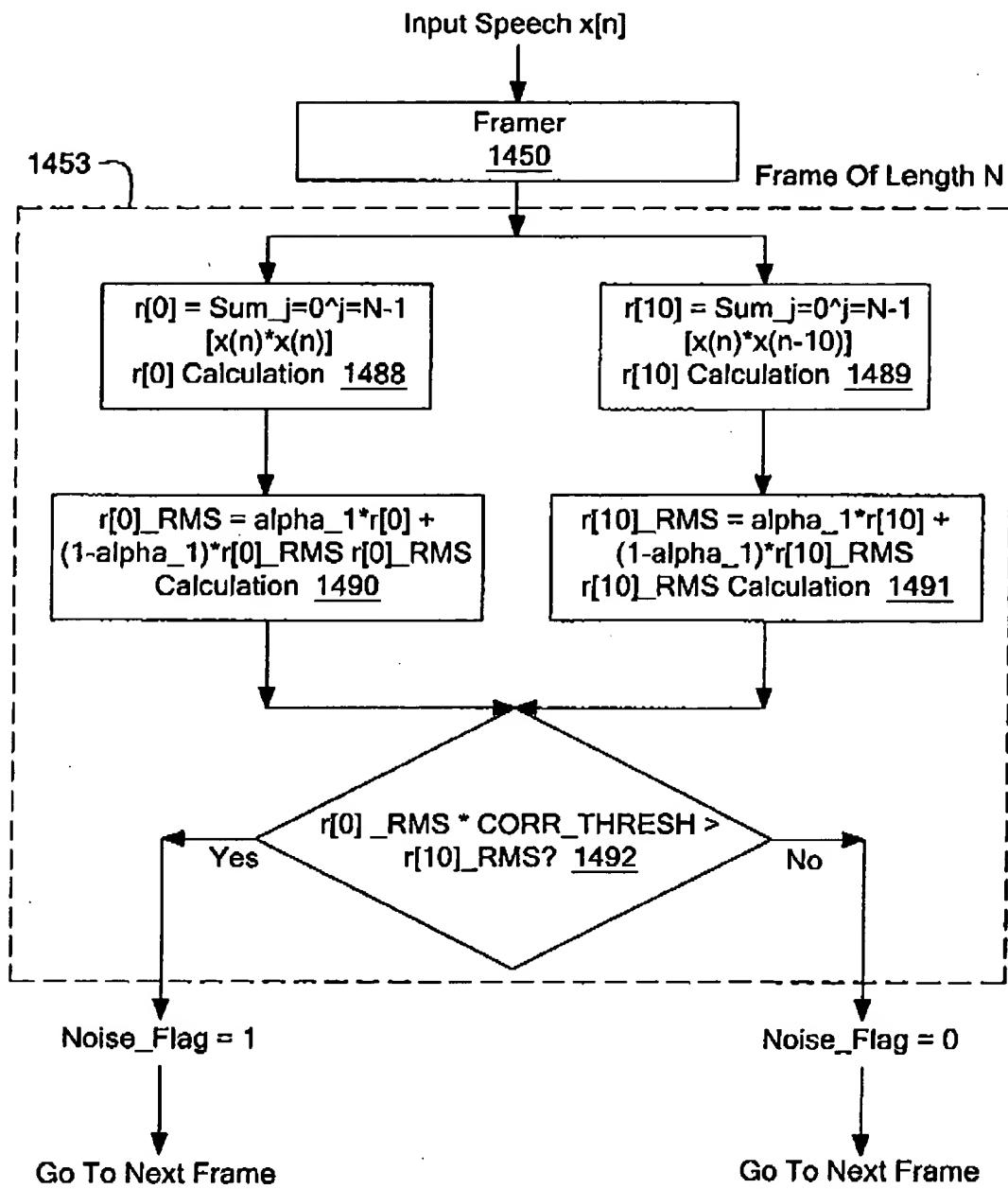


FIG. 14E

Replacement Sheet 09/938 104

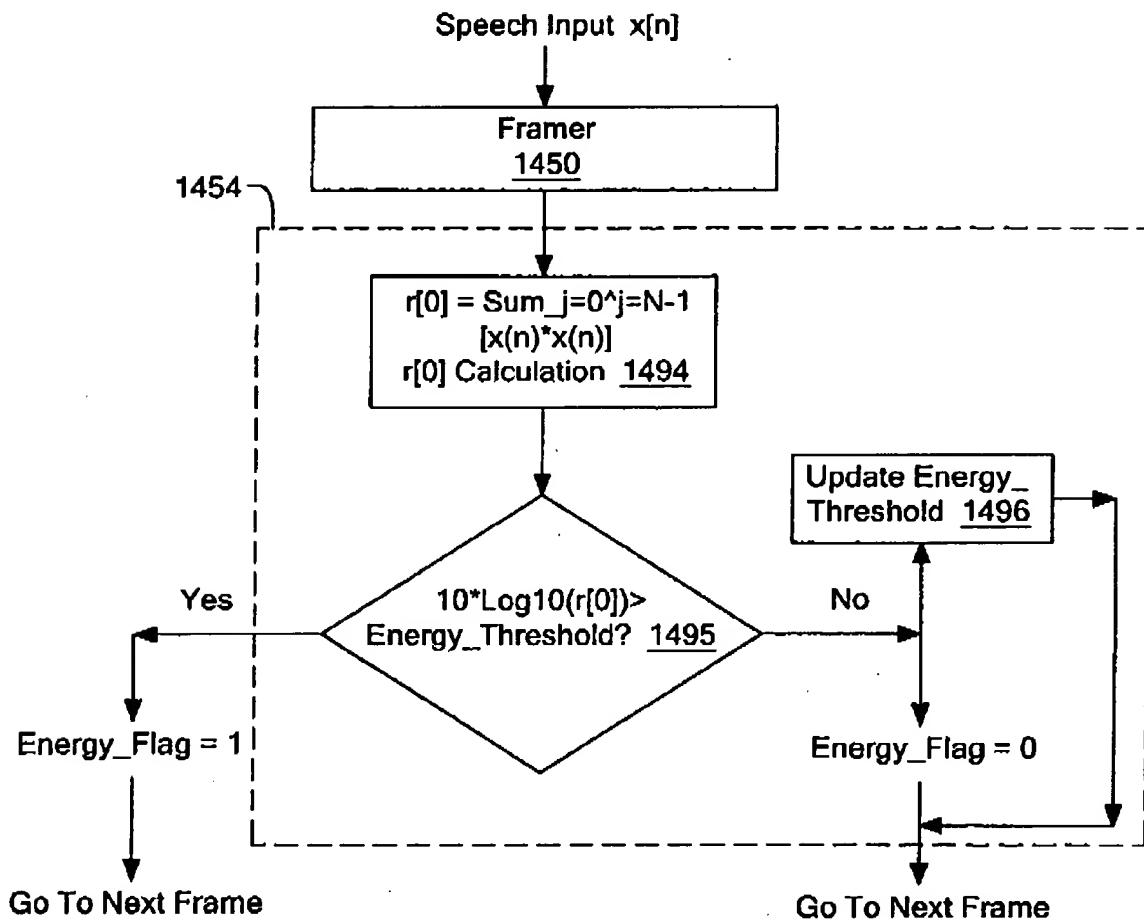
Energy Discriminator 1454

FIG. 14F

## Replacement Sheet 09/938104

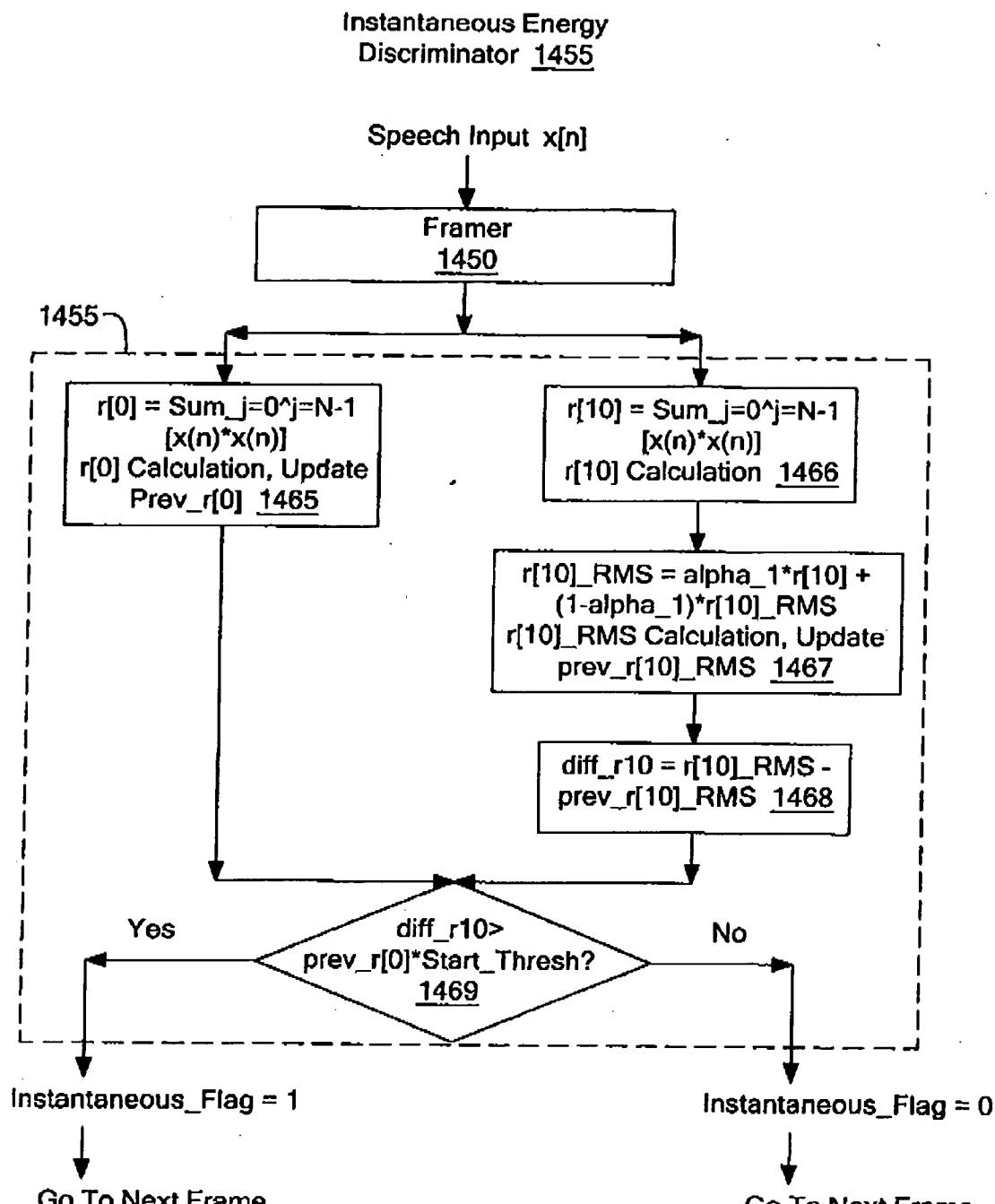


FIG. 14G

Replacement Sheet 09/938104

210

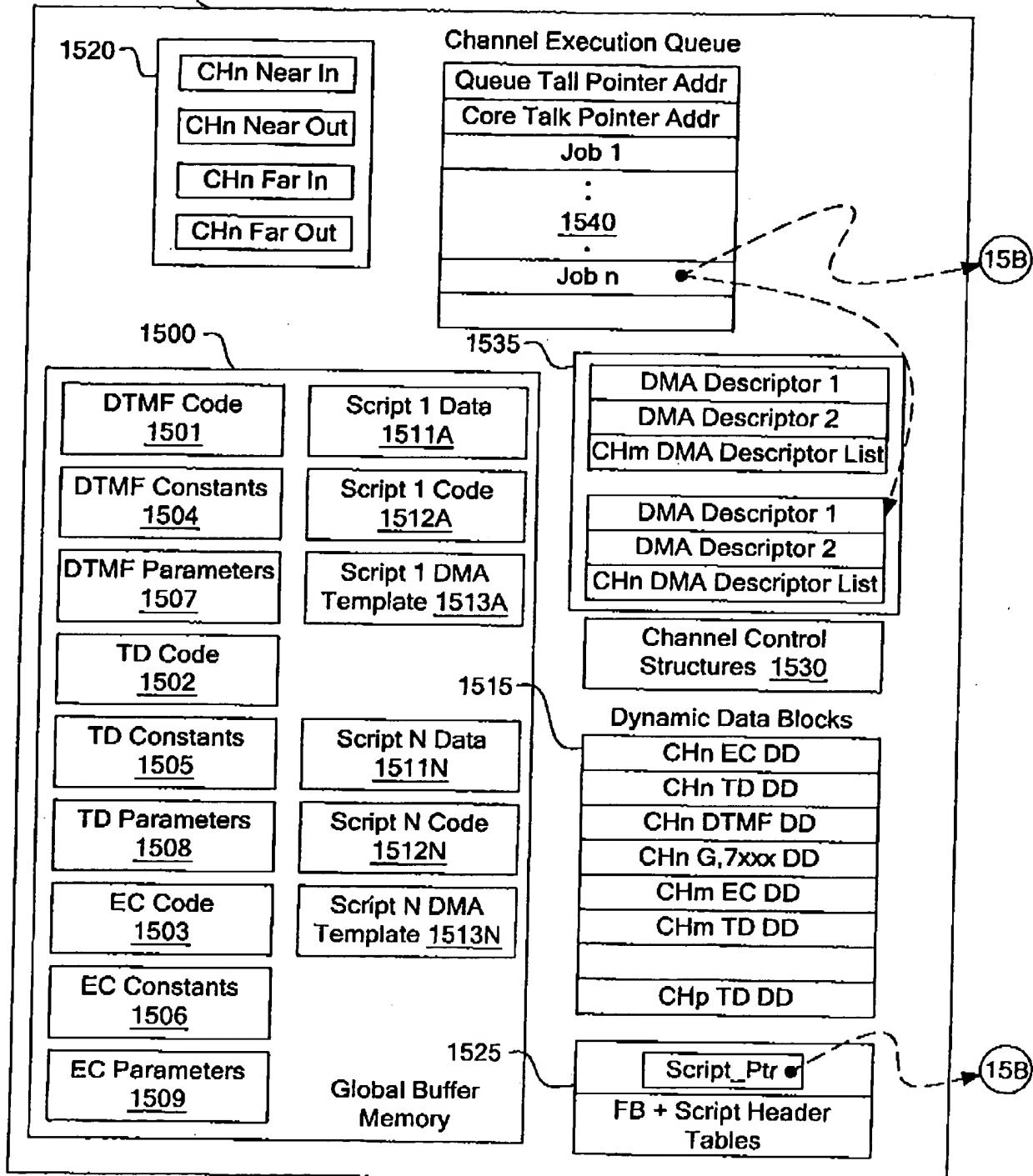


FIG. 15A

Replacement Sheet 09/938 104

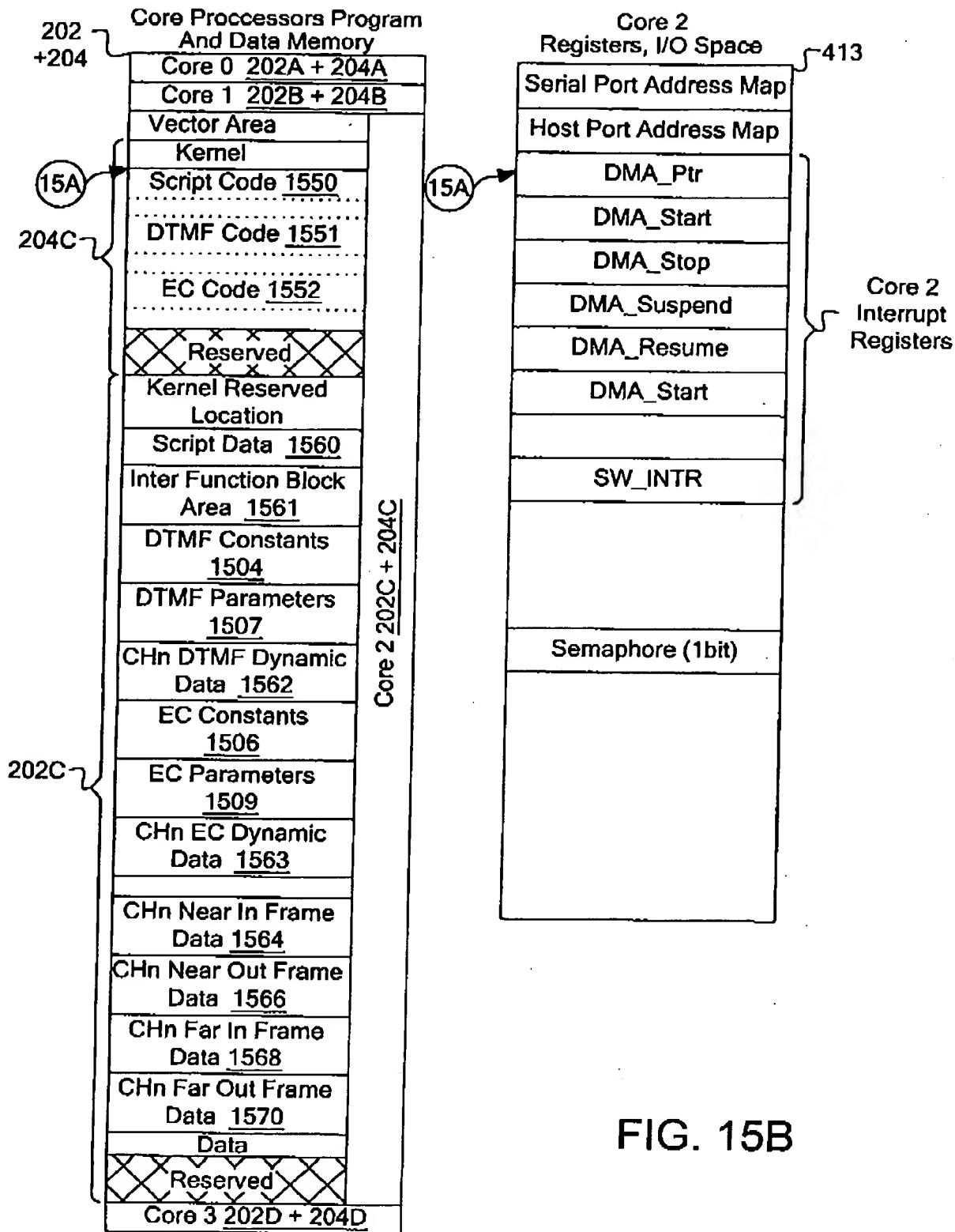


FIG. 15B

## Replacement Sheet 09/938104

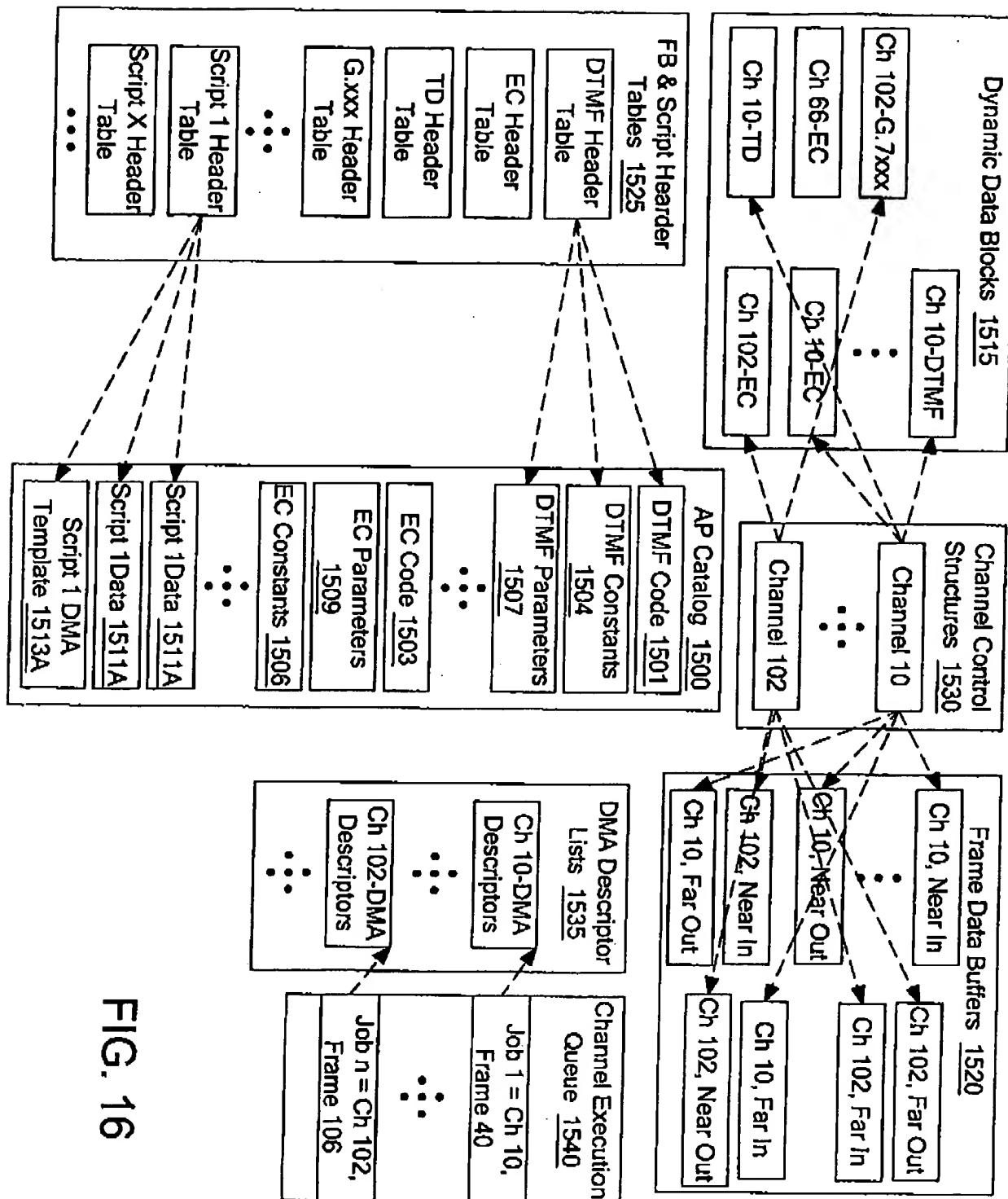


FIG. 16

Replacement Sheet 09/938104

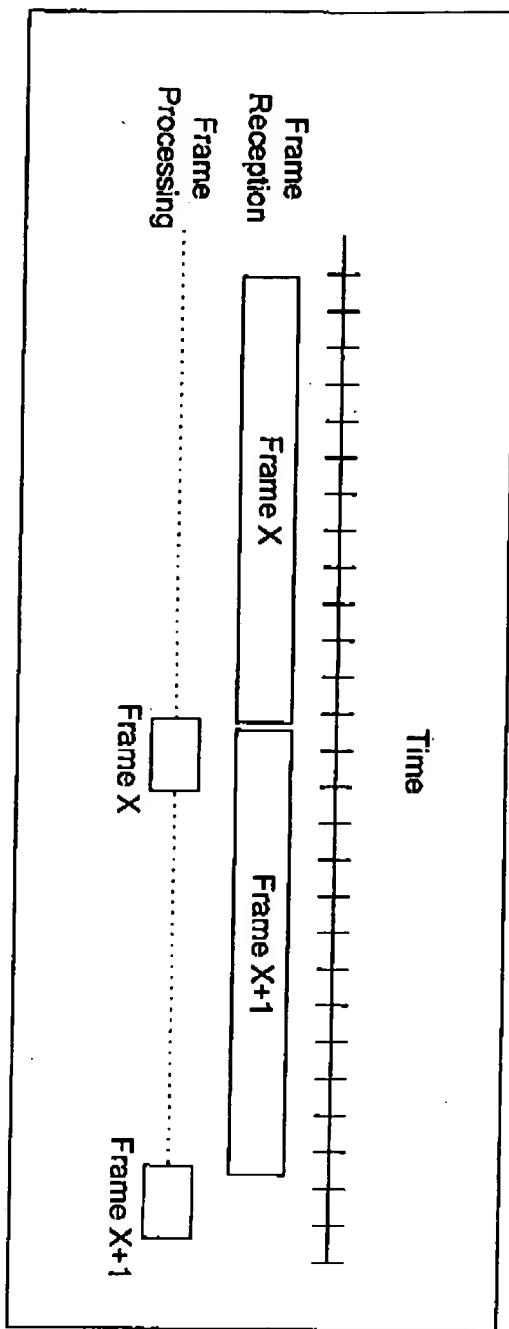


FIG. 17

Replacement Sheet 09/938 104

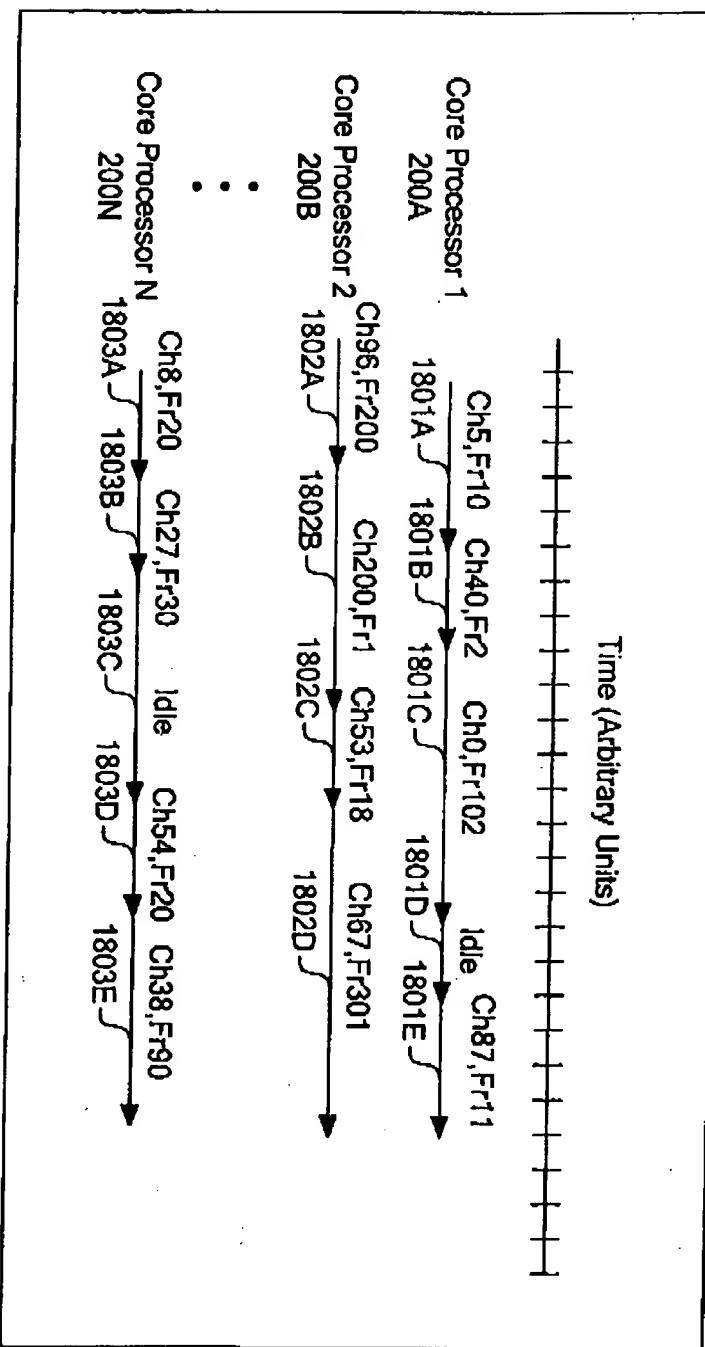


FIG. 18